

## REMARKS

Reconsideration of this application as amended is respectfully requested.

Claims 1-4, and 12-14 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,128,318 to Sato ("Sato").

Claims 5-11 and 15-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form.

Claims 23-44 are newly presented. It is respectfully submitted that no new matter has been added.

### Rejections under 35 U.S.C. §102(e)

The Examiner has rejected claims 1-4, and 12-14 under 35 U.S.C. §102(e) as being anticipated by Sato. Applicants submit that claims 1-4, and 12-14 are not anticipated by Sato. In regard to the rejection of claim 1, the Examiner has stated in part that:

"the claimed maintaining a synchronization state of a number of components of a distributed system is anticipated by method of synchronizing a "global" cycle master node (Figure 1, element 22) to cycle slave nodes (element 20) in a network. See column 1, lines 35-39 and lines 66-67, column 2, line 1, and column 4, lines 7-14. The claimed synchronization according to a number local clock cycles recorded between successive occurrences of a global synchronization signal provided to the components is anticipated by cycle reset signal asserted at a prescribed rate which is a multiple of one cycle slave node. (1/28/03, Office Action, p. 2)

Applicants respectfully submit that claim 1 is not anticipated by Sato. Claim 1 recites the features of "a number of local clock cycles recorded between successive occurrences of a global synchronization signal provided to each of the components within the distributed system." (Emphasis added) Sato does not disclose these features as can be seen by the following analysis of Sato. Sato discloses a method for synchronizing a cycle master node to a cycle slave node (not a cycle slave node to a cycle master node) using synchronization information from an external network. (Sato, title) Although Sato does

describe synchronizing local cycle masters with a global cycle master in his background (Sato, col. 1, ll. 36-39), he does not describe how this is done because it is not the subject of his invention. What Sato does describe is how a cycle slave node becomes the cycle master by synchronizing a cycle master node (located in a bridge) to the cycle slave node (located outside the bridge). (Sato, col. 1, ll. 55-62). Sato accomplishes this by implementing a control algorithm using an external synchronous cycle reset signal at the slave node, calculating a timer offset value equal to the difference between the slave's local timer value and the reset signal, and providing this timer offset value to the cycle master node. (Sato, col. 4, ll. 35-67). Sato's control algorithm (which allows a cycle slave node to be the master and allows the master to be slave node), therefore, does not provide for a synchronization state that indicates that the local clock generating circuit is synchronized to the global synchronization signal. (Claim 1, emphasis added)

Furthermore, applicants respectfully disagree with the Examiner that Sato's cycle reset signal asserted at a prescribed rate anticipates applicants' global synchronization signal. In fact, Sato describes that one of the cycle slave nodes in the network or sub-network, shown as the cycle slave node 20 in FIG. 1, receives the synchronous timer reset signal. (Sato, col. 4, ll. 15-20) In contrast, Sato describes a cycle timer value that is regularly distributed by a cycle master node to all the other nodes. (Sato, col. 4, ll. 7-14) However, Sato does not use the cycle timer value to implement his algorithm, but instead synchronizes a cycle master to a cycle slave's timer reset value as described above. Therefore, Sato's cycle reset signal does not describe a global synchronization signal provided to each of the components within the distributed system.

Because Sato neither describes "a synchronization state that indicates that the local clock generating circuit is synchronized with the global synchronization signal" nor "a global

synchronization signal provided to each of the components within the distributed system” as taught by claim 1, from which claims 2-11 depend, applicants respectfully submit that claims 1-11 are not anticipated under 35 U.S.C. §102(e) by Sato.

The Examiner also rejected independent claim 12 under 35 U.S.C. §102(e) for the reason set forth in the rejection of claim 1. Claim 12 discloses substantially similar limitations as claim 1, and recites “a synchronization state that indicates that the local clock generating circuit is synchronized to the global synchronization signal” nor “a global synchronization signal provided to each of the components within the distributed system.” (Emphasis added) Because, Sato does not disclose these features as taught by applicants’ claim 12 from which claims 13-22 depend, for the reasons discussed above with regard to claim 1, applicants respectfully submit that claims 12-22 are not anticipated under 35 U.S.C. §102(e) by Sato.

For the foregoing reasons, applicant respectfully submits that the applicable objections and rejections have been overcome and that the claims are in condition for allowance.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: April 25, 2003

Sanjeet Dutta

Sanjeet K. Dutta

Reg. No. 46,145

12400 Wilshire Boulevard  
Seventh Floor  
Los Angeles, CA 90025-1026  
(408) 947-8200